Remarks

Favorable consideration of the application is respectfully requested. Claims 1-20, prior to this paper, were pending in the present application. Claims 11-19 are withdrawn and claims 1-10 and 20 are rejected.

Claim Rejections - 35 U.S.C. §102

Claims 1-3 and 5-6, prior to this paper, were rejected under 35 U.S.C. §102(b) as being anticipated by Nishioka et al. (U.S. Patent 5,994,733).

The Examiner's rejection of claims 1-3 and 5-6, under 35 U.S.C. §102(b) as being anticipated by Nishioka et al. (U.S. Patent 5,994,733), is respectfully traversed. For a reference to be a proper §102 reference, each and every element or step of the rejected claim must be taught in a single reference. In light of the invention as recited in claims 1-3 and 5-6, Nishioka et al. does not meet this requirement as presented in the following discussion.

In claims 1 and 5, features of the present invention are recited as:

> "forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween and spanning completely between neighboring gate electrodes."

The Examiner references FIG. 2B of Nishioka et al. as anticipating the above recited feature of the present invention. However, there are simply no illustrations in FIG. 2B, or in any of the other embodiments of Nishioka et al. that show a metal interconnect running a major length of the connected together source electrodes and making a substantially continuous contact therebetween.

Comparing FIGS. 9 and 10 of the present application to FIG. 2B of Nishioka et al., the present application shows a metal interconnect, formed by titanium nitride 81 and metal 83, running a major length of the connected together source electrodes (the source electrodes formed by implant region 41) and making a substantially continuous contact therebetween.

In FIG. 2B of Nishioka et al., the source electrode, formed by an impurity region 14, is surrounded by a p-type pocket region 15. The impurity region 14 is covered by overlying insulating layer 16 (Refer to column 11, line 49 through column 12, line 9). Obviously, neither p-type pocket region 15 or insulating layer 16 can physically function as a metal interconnect running a major length of the connected together source electrodes 41 and making a substantially continuous contact therebetween, as claimed in the present invention.

Clearly, Nishioka et al. is not a proper §102 reference, nor is Nishioka et al. an adequate §103 reference as clearly demonstrated from the above arguments. Therefore, it is requested that the §102(b) rejection of claims 1-3 and 5-6 over Nishioka et al. be withdrawn and that claims 1-3 and 5-6 be allowed.

Claim Rejections - 35 U.S.C. §103

Claims 4, 7-10 and 20, prior to this paper, were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. (U.S. Patent 5,994,733), in view of Watanabe et al. (IEDM, 98 pp. 975-978).

The Examiner's rejection of claims 4, 7-10 and 20, under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. (U.S. Patent 5,994,733), in view of Watanabe et al. (IEDM, 98 pp. 975-978), is respectfully traversed.

As argued above, clearly Nishioka et al. is not an adequate §103(a) reference as in FIG. 2B of Nishioka et al. the source electrode is formed by an impurity region 14, surrounded by a p-type

pocket region 15. The impurity region 14 is covered by overlying insulating layer 16 (Refer to column 11, line 49 through column 12, line 9). Obviously, neither p-type pocket region 15 or insulating layer 16 can physically function as a metal interconnect running a major length of the connected together source electrodes 41 and making a substantially continuous contact therebetween, as claimed in the present invention. Adding the disclosure of Watanabe et al. (hereinafter Watanabe), does nothing to render obvious the features of presently claimed invention recited as:

> "forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween and spanning completely between neighboring gate electrodes."

Furthermore, Watanabe discloses on page 975:

> "The number of metal sourcelines parallel to bitlines can be dramatically decreased due to low resistance of W Inter-connect compared to conventional diffused sourceline with self-aligned source structure."

Watanabe is stressing by the statement "due to low resistance of W inter-connect compared to conventional diffused sourceline with self-aligned source structure" that Watanabe is using a tungsten interconnect to each source electrode of each individual flash device in lieu of the conventional method of having a continuous source connection of flash devices by a diffusion source.

This point is reinforced by the illustration of Fig.1(b) of Watanabe where it is shown that the W Local Interconnect is running perpendicular to the source diffusion region and makes contact at each intersection of the source diffusion region and the W Local Interconnect.

Clearly, the combination of Nishioka et al. and Watanabe, will not produce the present invention as currently claimed. Nishioka et al. does not form a metal interconnect that spans completely between neighboring gates of floating gate devices, runs a major length of the connected together source electrodes 41 and makes a substantially continuous contact therebetween, and the tungsten local interconnect of Watanabe runs perpendicular to the source diffusion of the floating gate devices and obviously does not run a major length of source electrodes connected together by a conductive implant. In fact, the combination of Nishioka et al. and Watanabe appears to teach away from the presently claimed invention.

Clearly, it is impossible for the combination of Kamitani and Watanabe to develop a method to form the structure of the presently claimed invention recited in claim 7 as:

> "forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;
>
> forming a tungsten-based interconnect running a major length of said connected together source electrodes, said tungsten-based interconnect making a substantially continuous contact therebetween; and
>
> forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug connecting between a drain electrode of each said floating gate device and a digit line"

and recited in claim 10 as:

> "forming a series of floating gate devices having their source electrodes connected together by a conductively doped active area, said source electrodes

being self-aligned to their respective transistor gates of each said floating gate device;

forming a nitride barrier layer overlying each transistor gate;

forming a planarized insulation layer over said nitride barrier layer;

removing portions of said planarized insulation layer while using said nitride barrier layer to self-align an interconnect via to said source electrodes;

forming a tungsten-based interconnect into said interconnect via, said tungsten-based interconnect running a major length of said source electrodes and making contact therebetween; and

forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug self-aligned to and connected between a drain electrode of each said floating gate device and a digit line."

Therefore, as argued above, the rejection of claims 4, 7-10 and 20, under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. (U.S. Patent 5,994,733), in view of Watanabe et al. (IEDM, 98 pp. 975-978), has clearly has not been established. It is requested that the rejection of claims 4,7-10 and 20, under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. (U.S. Patent 5,994,733), in view of Watanabe et al. (IEDM, 98 pp. 975-978) be withdrawn and that claims 4, 7-10 and 20 be allowed over the art of record.

Additional Information

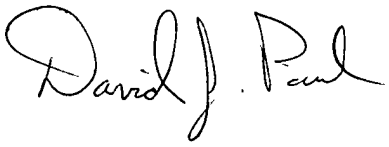
Relevant art cited on a co-pending application (U.S. Patent Application No. 09/905,517) for the assignee and inventor of record has been included for the Examiner's consideration. It is believed the present invention, as currently claimed, should be allowed over the currently cited art as well as the art of record.

Conclusion

Applicant submits that the application is in condition for allowance. Such allowance at an early date is respectfully requested.

To that end, if the Examiner feels that a conference will expedite the prosecution of this case, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,



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